IN THE CLAIMS:

1. (Currently Amended) A method for modifying processing ~~memory~~ on at least one control device, the method comprising:

transferring data from a remote host device to the at least one control device during unscheduled communications periods and without interrupting operation of the at least one control device, the remote host device and the at least one control device being coupled through a Fieldbus communications network;

storing the transferred data to a respective inactive memory area; and,

redirecting at least one control device microprocessor, during an idle period of the at least one control device microprocessor, to execute the stored data in the inactive memory area to modify the processing on the at least one control device.

2. (Previously Presented) A method according to claim 1, further comprising verifying the stored data in the respective inactive memory area.

3. (Previously Presented) A method according to claim 1, wherein redirecting the at least one control device microprocessor comprises providing the at least one control device microprocessor with entry points to the stored data.

4. (Previously Presented) A method according to claim 1, wherein transferring data comprises transmitting entry points.

5. (Previously Presented) A method according to claim 1, wherein transferring data comprises transmitting executable instructions.

6. (Previously Presented) A method according to claim 1, wherein transferring data comprises synchronizing data transmissions between the host device and the at least one control device to avoid interference with scheduled communications.

7. (Previously Presented) A method according to claim 1, further comprising:

selecting a respective at least one active memory area; and,

inactivating the respective selected active memory area such that the at least one control device microprocessor does not execute data in the respective selected active memory area.

8. (Previously Presented) A method according to claim 1, wherein redirecting the at least one control device microprocessor comprises issuing an upgrade request from the host device to the at least one control device.

9. (Previously Presented) A method according to claim 8, wherein issuing an upgrade request comprises coordinating at least one upgrade command from the host device to the at least one control device.

10. (Previously Presented) A method according to claim 1, wherein redirecting the at least one control device microprocessor comprises:

monitoring at least one parameter; and,

communicating a command to redirect the at least one control device microprocessor when the parameter attains a specified value.

11. (Currently Amended) A system for modifying processing ~~memory~~ on at least one control device, the system comprising:

a remote host device coupled through a Fieldbus communications network to the at least one control device and configured to transfer data to the at least one control device during unscheduled communications periods and without interrupting operation of the at least one control device, and

at least one control device including:

at least one active memory area and at least one inactive memory area;

at least one control device microprocessor to execute instructions and data in the at least one active memory area; and,

a control device selector module to direct the at least one control device microprocessor to the at least one active memory area, the selector module further comprising a scheduling module to redirect the at least one control device microprocessor during microprocessor idle periods to modify the processing on the at least one control device.

12. (Previously Presented) A system according to claim 11, wherein the selector module comprises entry points to direct the at least one control device microprocessor.

13. (Previously Presented) A system according to claim 11, wherein the at least one control device microprocessor comprises a memory verification module.

14. (Previously Presented) A system according to claim 11, wherein:

the at least one active memory area comprises flash memory; and,

the at least one inactive memory area comprises flash memory.

15. (Previously Presented) A system according to claim 11, wherein the remote host device comprises:

a Fieldbus communications module to access the Fieldbus communications network;

a control module to receive, transmit, and display commands and data between the Fieldbus communications network and a host device user; and,

a control device communications module to transmit and receive commands and data between the host device and the at least one control device.

16. (Original) A system according to claim 15, wherein the control module further comprises a user interface.

17. (Original) A system according to claim 11, wherein the host device is a microprocessor-based device.

18. (Original) A system according to claim 11, wherein:

the active memory data comprises executable instructions and data; and,

the inactive memory data comprises executable instructions and data.

19. (New) A method of implementing a software upgrade for a control device, the method comprising:

transferring, without interrupting operation of the control device, software upgrade data from a remote host device to the control device during unscheduled communications periods between the control device and control equipment of at least one process controlled by the control device, the remote host device and the control device being coupled through a Fieldbus communications network;

storing the upgrade data to a respective inactive memory area; and,

redirecting at least one microprocessor of the control device, during an idle period of the at least one microprocessor, to execute the stored upgrade data in the inactive memory area to implement the software upgrade for a next active period of the microprocessor.

20. (New) A method according to claim 19, wherein:

transferring upgrade data comprises transmitting executable instructions and entry points to the instructions; and

redirecting the at least one microprocessor comprises providing the at least one microprocessor with the entry points.